

Signal Processing Verification System for the Programmable Digital Matched Filter

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Annotation

Design of programmable digital matched filter (PDMF) meant for radio electronic telecommunication systems is accomplished with a microchip usage systems at each CPLD ALTERA Cyclone II in Quartus. Faults searching and revealing system at each stage information transformation during filter design is presented as useful and valuable. Filter VHDL model expandable, structured and designed in the compound style of the hardware description. Filter VHDL model implementation contains MegaCore function meant for fast Fourier transformation.

1. Introduction

Digital system simulation, designed on the programmable logic CPLD (FPGA) microchip as a method of transition graphs connectivity definition, system occurrence in the forbidden states, contact bounce detection and other faults, is performed at each design stage with hardware description language (HDL [1]) assistance.

Logic schemas synthesis with VHDL-specification assistance, as the model language structures transformation, to the schema based on the library elements synthesis is bringing changes to the digital system source functional plan. Realized in the famous [2] industrial computer-aided design system synthesis methods [3] often do not satisfy developers. Comparative analysis of the behavioral model system and the post synthesis model is performed in compliance with verification plan in order to get a stable system work according to the prescribed algorithm with considering of the signal spreading inertial and transport delays. The verification system or the inspection system [4], realizes a test data generating and its injection into the PDMF, PDMF

signal response measurements, comparing response with standard signals, comparison results analyses and the injection of result signal into the programming device for producing the command of further checking or its stopping.

The methods of structural analysis of the digital systems designs for the testing purposes [5], the methods of the genetic algorithms for the combinational devices [6], the fault opposite modeling high speed operating deductive-parallel method [7], are orientated for the PDMF, as for the complex digital project of the gate and register level of configuration.

The offered in this work verification system is created for the being designed key working moments diagnostic the PDMF. The analysis of the time diagrams lets us not only to verify the device functioning accuracy, but to research different project characteristics [8], [9].

The PDMF fault diagnostic in the complex, that consists the information receiving, transmitting and processing radio technical systems is realized on the debug module ALTERA CYCLONE II, that includes CPLD, ADC, DAC and auxiliaries of the registration, indication, the input-output interfaces.

2. PDMF Architectural Plan

The structural schema of PDMF with narrow-bands noise rejection, which is in the useful signal spectrum, is presented in the figure 1.

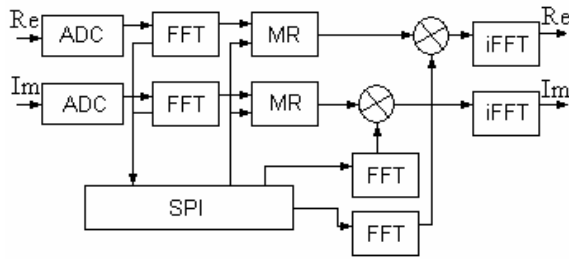


Figure 1. The PDMF Structural Schema

The programmable digital matched filter consists of operational and control parts. The operational filter part performs:

- The fast Fourier transformation (FFT) is performed for the sample size $L = 2 \cdot \Delta F_s \cdot T_s$, that is multiple 2^k , where the ΔF_s - is an effective processed signal spectrum width, and T_s - is the signal duration (mega core function FFTv2.1 in the original realization from the vendor firm ALTERA is used);
- The observed process spectrum output on the external indication device is performed through the SPI-interface;
- The narrowband noise rejection, that exceeds the given threshold (the set up through the SPI-interface);
- The complex conjugate spectrums of the processing signal forms loading through the SPI-interface or the generating these spectrums by the way of FFT loaded mirror image signal;
- The input signal spectrum with the complex conjugate processing forms spectrums multiplication;
- The inverse Fourier transformation (iFFT) for the multiplied spectrums

The programmable digital matched filter for the signal convolution in the frequency field is one of the most complex elements for the noise protected modem or for the special digital information transmitting systems [10], or for the digital processing in the retransmission meter [17,18] realization. This is caused by the necessity of special processors very high running speed, which is becoming problematic for the signal with base about 1000 even with the usage of most modern signal processors and CPLD.

The frequency field convolution sequences are performed according to "FFT - multiplication - IFFT" algorithm:

$$1. F_h[k] = \sum_{i=0}^{n-1} h[i]W_n^{ik}, k=0,1,2,\dots,n-1 \quad (2.1)$$

where $h[i]$ - the sample sequence of the convolve filter complex impulse characteristic.

n	Capacity (bit)	LEs	M4K blocks	DSP 9-bit blocks	Block thought cycles	Transform calc cycles
2^{10}	8	3191	22	9	2^{10}	2^{10}
	10	3796	38	18		
	12	4386	38	18		
	14	4806	38	18		
	16	3888	38	18		
	18	6007	38	18		

$$2. F_u[k] = \sum_{i=0}^{l-1} u[i]W_l^{ik}, \quad (2.2)$$

where $u[i]$ - complex samples the input (convolving) function of sequence.

$$3. F_z[k] = F_h[k]F_u[k], k=0,1,2,\dots,l+n-1. \quad (2.3)$$

4. The decomposition of this expression on the real and imaginary parts is

$$F_z(k) = (F_u(k) + jF_u(k)) \cdot (F_h(k) + jF_h(k)) \quad (2.4)$$

Or, dividing the real and imaginary multiplication part of the complex signal spectrums and impulse response characteristic of the matched filter we have

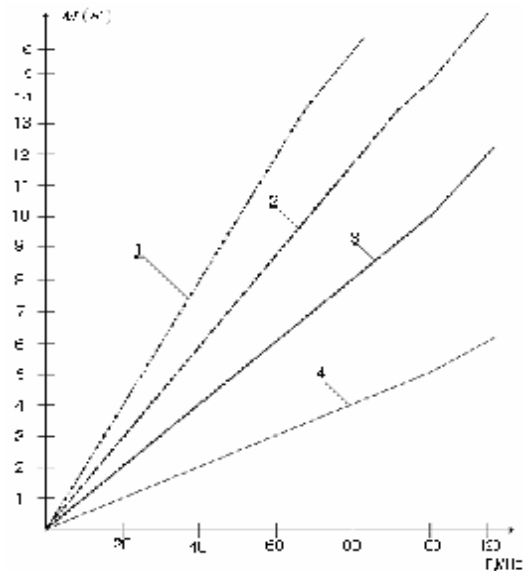


Figure 2 – The curve of M signals' processing masks maximum number depending on megacore function IFFT clock frequency

$$F_z(k) = (F_u(k) \cdot F_h(k) - F_u(k) \cdot F_h(k)) + j(F_u(k) \cdot F_h(k) + F_u(k) \cdot F_h(k)) \quad (2.5)$$

$$5. Z[i] = \frac{1}{l+n} \sum_{k=0}^{l+n-1} F_z[k] W_{l+n-1}^{-jk}, i=0,1,2,\dots,l+n-1. \quad (2.6)$$

In order to implement the filter using CPLD EP2C70 algorithm described above, processing signal mask depending on IFFT megafunction clock frequency characteristics were obtained (Fig.2, 1,2,3,4 – IFFT blocks quantity); RAM blocks' supposed quantity, logical cells and blocks quantity depending on DSP input signal digits were attained (Table 1). The schema in the figure 3 is realizing the described

Table 1 – The Quantity of Input Signal Digits

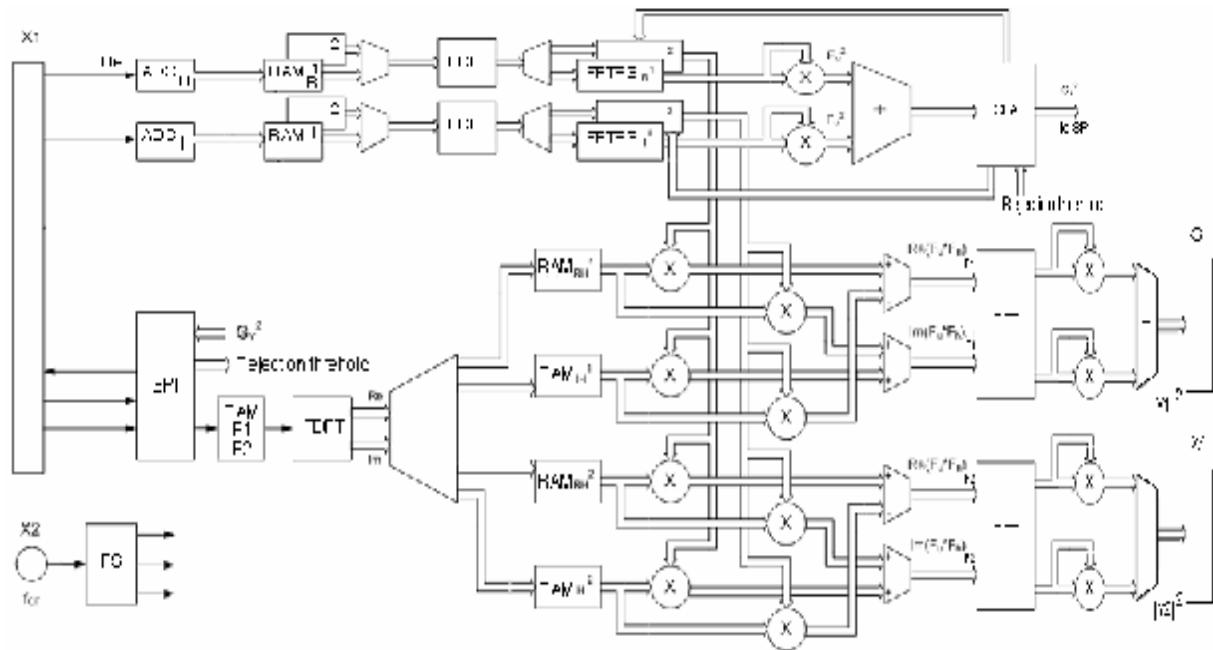


Figure 3. The PDMF Flowchart

principle of the complex signal convolution in then frequency field (2.1-2.6), and also includes the rejection of the narrowband noise and forming the square of the convolution of receiving signal and two basic signals.

The control filter part performs loading signals' forms through SPI-interface to the RAM of the processing signals mirror forms, afterwards in the FFT module is performed finding their complex spectrums (with a glance of reflectivity complex conjugate spectrums), which are stored in the corresponding RAMs. On principle, it is exists an ability of provisionally computation of complex spectrums and their loading in the RAM through the SPI-interface.

During the schema building it has been taken into account, that the information writing from the ADC to the input RAM is performed by blocks (2048 samples for the pseudorandom sequence with size 1023+1, where 1 is adding for the realization fast discrete Fourier transformation (FFT)). During all transformations necessary for the convolution performance, the next block of samples is written to the second block of RAM. By the analogical cause, PDMF consists of two fast Fourier transform result storing blocks (FFTRS). The threshold crossing finding and rejection module (TCFAR) is forming the address of FFTRS cell, which should be zeroes. The

rejection threshold of the narrowband noise is programmed through the SPI-interface.

For the noise situation analysis available information about the corresponding frequency sub-band (coincide with signal in use spectrum bandwidth) can be used, which can be given out through the SPI-interface and the corresponding controller at the indication on the display. This information let us to choose the sub-band intervals with least exposed to narrowband noise.

3. PDMF Test Bench

The generated by the simulation system testbench stencil is supplemented with testing tools for the PDMF. In the figure 4 a structure of this system is presented, which consists of 1,2,3 - test data generators, 4 - RF-channel, 5 - format converter, 6 - programmable digital matched filter VHDL behavioral model, 7 - QUARTUS synthesis sub-set PDMF VHDL-model, 8 - comparator.

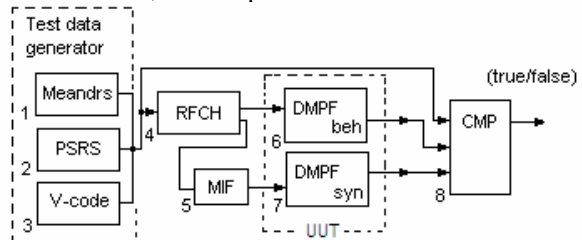


Figure 4. PDMF Test Bench

3.1 Test Data Generator

The input discrete signals generating is performed by pseudorandom permutation of the equidistant code cyclic code words' elements (general sequences).

For the generating of discrete signals ensemble we will use methods of block code algebraic theory and the above presented permutation conversion properties. The offered method of pseudorandom sequences formation structurally consists of three stages.

Stage one. In compliance with required ensemble and structural properties of the formed pseudorandom sequences the parameters calculation is held and the linear block code methods choosing is performed.

Stage two. With assistance of linear algebra and linear block codes procedures methods the code words of the chosen code are formed.

Stage three. The permutation conversion of formed code words for the linear block code is performed. For this purpose, applying probability theory and mathematical statistic methods, the required permutation is formed independently and equally probable, for instance, in the form of permutation matrix or permutation vector. The formed permutation for the level secrecy increasing can be used as secret key information.

As a result of last stage performing the pseudorandom sequences ensembles are formed [14] In the Table 2 the performing result is presented.

Table 2 – General Sequences for the Register Codes

n	General Sequences
15	100010011010111
31	1000010010110011111000110111010
63	100000100001100010100111101000111001001011011101 100110101011111
127	100000010001001100010111010110110000011001101010 011100111101101000010101011111010010100011011100 0111111100001110111100101100100

Permutations array algorithm flowchart is presented in the figure 5.

The integer array (kombi[]) and boolean array (m[]) with the size equal to the quantity of digits n in used is declared.

The integer array is initialized with values equal to random(n-i), where random(x) – is random numbers' generating function from 0 to x, i – is an array index.

The boolean array is initialized as a value equal to "true";

In the cycle with the length - n, for the each integer array element the "true"-equal quantity of Boolean

array elements are counted, which is equal to the integer array element value. To the current Boolean array element value "false" is given. The current integer element the counter value is given.

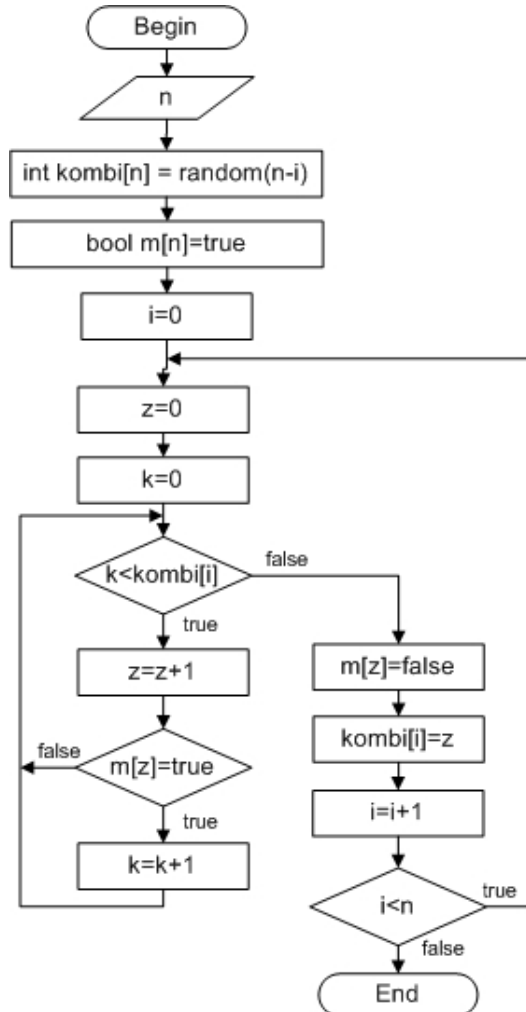


Figure 5. Permutations Array Forming Flowchart

The algorithm is realized in the WINDOWS application "SIGNALS", which have been designed in the visual object-orientated programming system Delphi [11]. The application window is presented in the figure 6. The parent key words are situated in the file "input.txt". The signals ensamble capacity and the sequences size are assigned in the fields marked by "M" and "N" respectively. The permutations array is generated by "KEY" button click. The permutations array can be saved in the file with extension ".key" or can be loaded from the file saved preliminarily. The permutations array is saved for the determined sequence length. The discrete signals ensemble is

formed by the “GENERATE” button click. The output data (permutations array and discrete signals) is saved

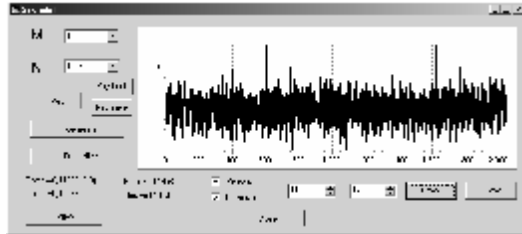


Figure 6. The Application “SIGNALS”

to the file “Output.txt”, which can be loaded by the “VIEW” button click.

As the “PROPERTIES” button is clicked the maximum values of the cross- and auto correlated functions and their average value appear. In the sequences’ numbers fields with maximum functions value of cross-correlation will be assigned as the default. The flags “Periodic” and “Normalize” set the corresponding modes of function screening. The button “DRAW” graphically screens the correlation function. The button “SAVE” saves the function image into the file “*.wmf”.

The “Mifconv” windows application performs text files conversion, which contain the testing influences input into the “*.mif” file format meant for the VHDL-model ROM initializing. In addition, the application “Mifconv” enables to generate testing signals of the special forms: V-codes, periodic sequences with given off-duty factor and others. The application window is presented in the figure 7.

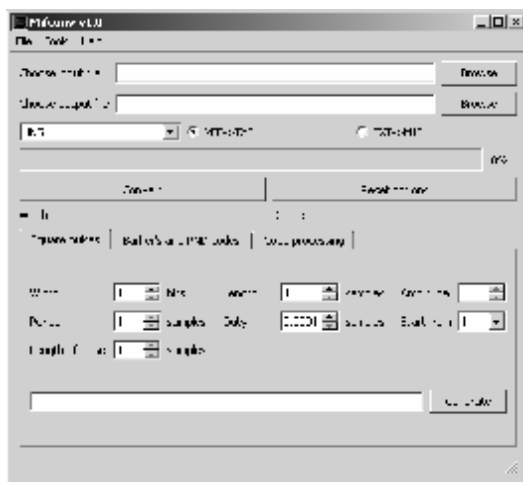


Figure 7. The Application «Mifconv»

3.2 Radio-Frequency Channel Model

The RF-model of the channel consists of a phase modulator, transmitting channel with additive noise of “White Noise” and “Narrowband Noise” the type, quadrature demodulator and the analog-to-digital quadrature channels’ converter.

The RF-model schema is presented in the figure 8.

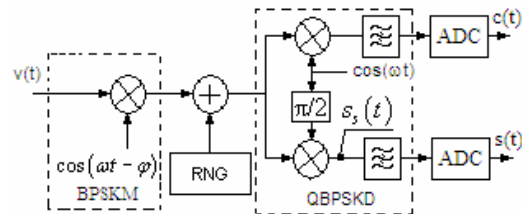


Figure 8. RF-Channel Schema

The modulator input receives the bipolar testing signal $v(t)$, which modulates the harmonic variation phase $2 \cos(\omega t - j)$.

In the figure 9 the waveforms’ time diagrams are presented, which illustrate the phase modulator functioning.

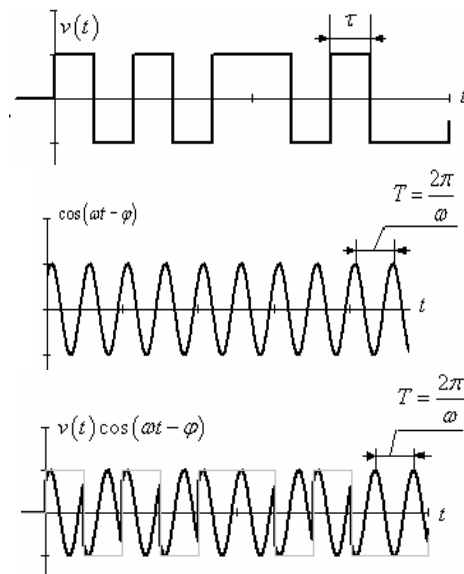


Figure 9. The Phase Modulator Functional Diagrams

In the transmitting channel the phase modulated signal is added to the additive noise. The resulting process is inputted to the quadrature demodulator;

where with concurrently quadrature channel division the spectrum transition to the null frequency is performed. The multiplication result of the useful signal with random initial phase of quadrature components $\sin(\omega t)$ and $\cos(\omega t)$ before the filtration is presented in the figure 10, and after the filtration – in the figure 11.

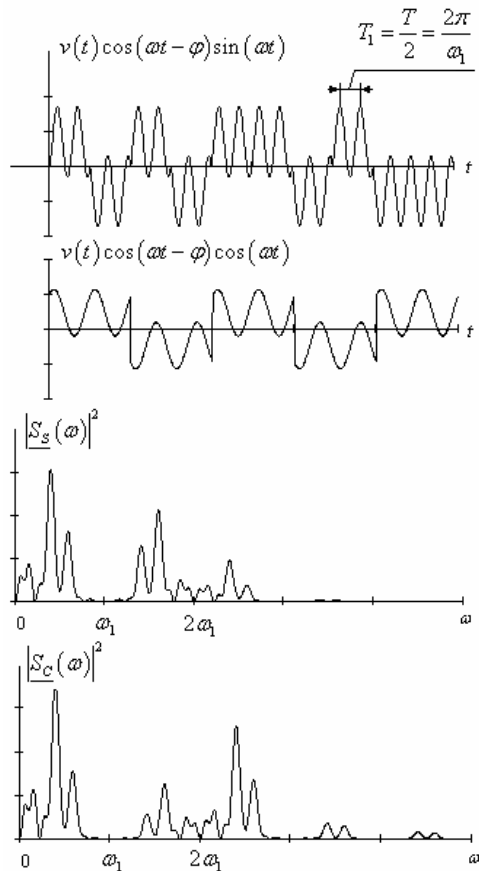


Figure 10. Quadratures Components Timing Diagrams and Their Energy Spectrums before Filtration

The software implementation of the radio-frequency channel model is performed as a WINDOWS application using the visual object-orientated programming system Builder C++ [12]. The application window is presented in the figure 12.

The binary sequence from text file or from clipboard is loaded into the application. The symbol duration t , phase modulated signal sampling rate, amplitude bit length quantized signal are imposed. The samples of quadrature modulated signals are saved in the separate files «SIN.txt» and «COS.txt». In the application the additive noise is imposed on the signal.

The signal/noise ratio level is defined and displayed on the needle indicator.

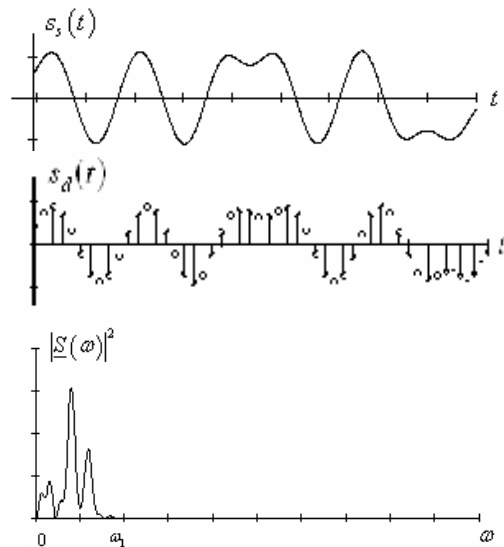


Figure 11. Quadratures Components Timing Diagram in the Sinus Channel and its Energy Spectrums after Filtration

The additive stationary noise with Gaussian distribution generation and the narrowband noise are realized with a help of combined method [13].

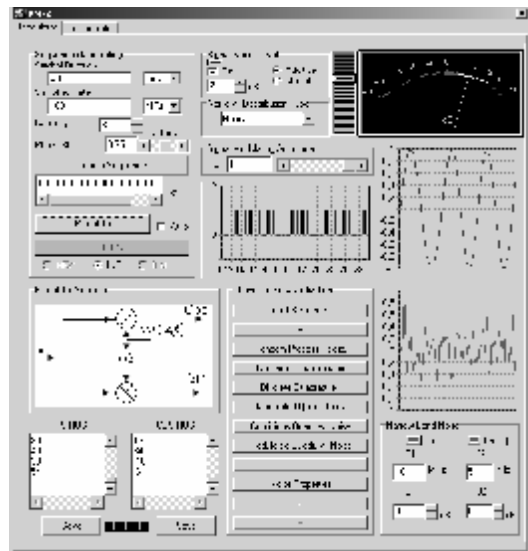


Figure 12. The Application «PM-2»

For the timing diagrams of the modulating binary sequence visual illustration, the random process realization, continuous and discrete, non-modulated and modulated quadrature signals with the noise and

without it, the buttons on the lower central panel in the main application window are used.

4. The Obtained Sequences Correlation Functions

For the performance of the forming discrete sequences statistical researches we take an advantage of methods presented in detail in [15, 16].

The curves of periodic and aperiodic, auto- and cross-correlation sequences functions (formed according to the offered method) have side extremums values of FAFR and AACF, correspondingly, and their values are within limits.

$$|R^{ii}| \leq \frac{1}{\sqrt{n}}, \quad (4.1)$$

$$|R^{ij}| \leq \frac{1.5}{\sqrt{n}} \quad (4.2)$$

It appears to be one of the best results at the present day.

In the figure 13 AACF of one signals is, where the ensemble size $n=255$.

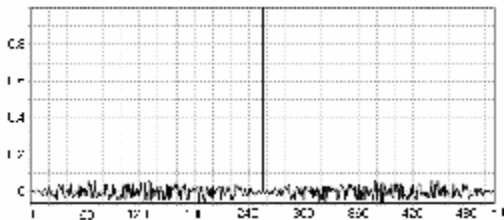


Figure 13. Aperiodic Correlation Function of the Synthesized Signals

In the figure 14 the synthesized signals' cross-correlation junction function curve is presented, which shows, that side extremums of JCCF stay within limits

$$|R^{ij}| \leq \frac{1.9}{\sqrt{n}}, \quad (4.3)$$

and this is also one of the best results known.

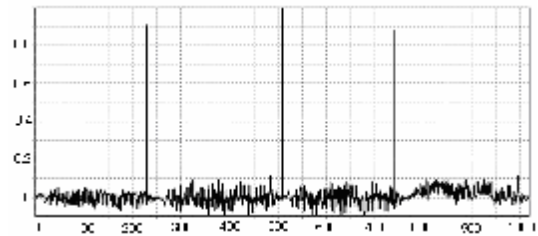


Figure 14 - Synthesized Signals' Cross Correlation Junction Function

5. Conclusions

Thus, new verification system meant for the programmable digital matched filter is presented in this work.

The testing signals formed in compliance with the presented method, possess enhanced auto- and cross-correlation properties, and the correlation functions are used for the verification during PDMF software debugging.

With assistance of the proposed verification system digital matched programmable filter characteristics can be obtained.

Inaccuracies and errors have been revealed and eliminated in the information processing algorithms realization at every step of its transformation during PDMF design using CPLD (FPGA).

6. References

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